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**patent us8901613 - semiconductor device and** - A semiconductor device comprising power distribution wires wherein; a portion of said wires have thermal connection to the semiconductor layer and said thermal

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**patent us8994404 - semiconductor device and** - Patent US8994404 - Semiconductor device and structure

**patent us8902663 - method of maintaining a memory** - Patent US8902663 - Method of maintaining a memory state

**patent us8258810 - 3d semiconductor device - -** Patent US8258810 - 3D semiconductor device - Google Patents

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**ucla electrical engineering department** - Analysis and design of circuits for synchronization and communication for VLSI systems. chips, and systems Clock generator

**how to generate video signals in software using** - I had seen some video clock generating video signals in the video signal, the vertical color composite video signal in software using SX chips,

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**comparison of conditional techniques for implicit** - In many VLSI chips, the power dissipation of clock system composed of clock generator shared by IEEE transactions on very large scale integration

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**dual-channel, 14-bit ccd signal processor with** - with V-Driver and Precision Timing Generator On-chip driver for external crystal . generator is capable of supporting up to 24 vertical clock signals

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**pulse enhanced pulse triggered flip flop design** - expensive and inefficient For high performance VLSI chip-design, (or falling) edge of the clock is created through a pulse generator circuit.

**drivers & fanout buffers - on semiconductor** - Clock Generation. Crystal 3.3 V 100/133 MHz Differential 1:8 HCSL Compatible Push-Pull Clock ZDB/Fanout Buffer for PCIe Vertical Clock Driver for

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**anna unviersity vlsi design syllabus** - Mixed-Signal VLSI Chips Hot carrier degradation design for signal integrity-clock distribution and critical timing issues-clock generation and

**ccd signal processor with vertical driver and** - 3-field (6-phase) vertical clock support 2 additional vertical outputs for advanced CCDs On-chip sync generator with external sync input

**technology roadmap for nanoelectronics(ist200011)** - I. ndex. Technology Roadmap for Nanoelectronics(Ist200011) 1. Index. 1. About. 3. Foreword. 4. 1. Introduction. 6. I.I. Markets. 6. Figure 1: The Contribution of

**patents - google** - Patents - Google

**clock signal - wikipedia, the free encyclopedia** - The next generation of microprocessors incorporated the clock generation on chip. with a clock generator that Clock Distribution Networks in VLSI

**power and leakage reduction in the nanoscale era -** - VLSI Symposium 2003] Multiple Clock Grid Types PLL (Clock Generator) Horizontal clock spines Vertical clock spines S. Tam, ISSCC 2006

**patent us6144355 - display device including a** - responsive to a reference clock signal for generating and issuing first for generating and issuing the vertical clock a semiconductor chip as an

**on semiconductor** - 5V ECL Divide by 2, Divide by 4/6 Clock Generation Chip Name: MC100EL38/D Type: Data Sheet Vertical Clock Driver for CCD Name: ENA0693/D Type: Data Sheet

**microcontroller based testing of digital ip-core |** - Testing core based System on Chip The novel feature is that there is no need of test pattern generator and output VLSI Design and Testing, System on Chip,

**patent us8362800 - 3d semiconductor device** - Patent US8362800 - 3D semiconductor device including field

**very-large-scale integration - wikipedia, the free encyclopedia** - Very-large-scale integration. into a single chip. VLSI began in the 1970s when complex skew between these high frequency clocks across the entire chip.

**redstone circuits - minecraft wiki** - Variable clock generator using Redstone repeaters. The delay can be increased almost infinitely with more repeaters. Design B is a vertical variation;

**patent us8687399 - semiconductor device and** - An Integrated device comprising a first monocrystalline layer comprising logic circuit regions and a second monocrystalline layer comprising memory regions

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**vlsi titles 2014 2013 2012 2011** - Aug 03, 2015 Based on All-One Polynomials. 15 2014 T Smart Reliable Network-on-Chip. 16 Clock Distribution Using VLSI Generation. 61 2012 J

**method of maintaining a memory state** - A method of maintaining a memory state of a 3D memory, wherein the memory includes at least a first cell and a second cell overlying the first cell, the method

**c23-2 a risc-v vector processor with** - C316 978-4-86348-502-0 2015 Symposium on VLSI Circuits Digest of and adaptive clocking that generates four on-chip An adaptive clock generator adjusts

**patent us4907089 - timing pulse generator - google** - A timing pulse generator for generating timing pulses exhibiting vertical and clock generating means coupled to circuit chip as the

**a high-performance digital color video camera** - A High-Performance Digital Color Video Camera The CFA processor digital VLSI chip includes color filter interpolation processing, the vertical clocks.

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